

FIG. 1

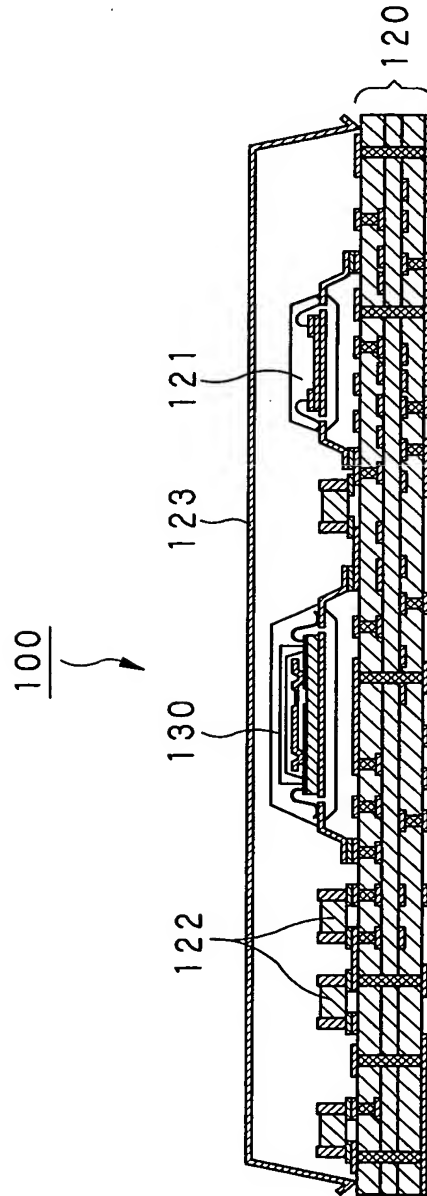


FIG.2

3/11

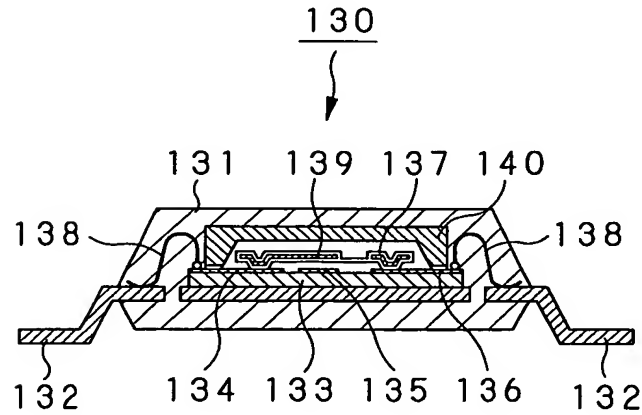


FIG. 3

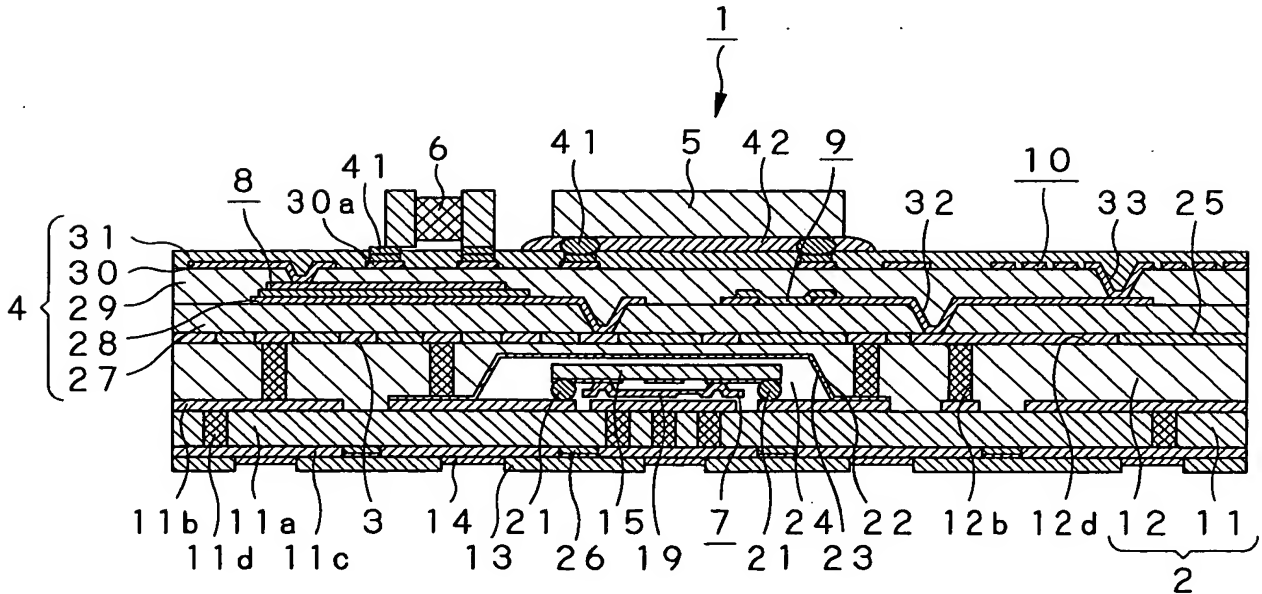


FIG. 4

4/11

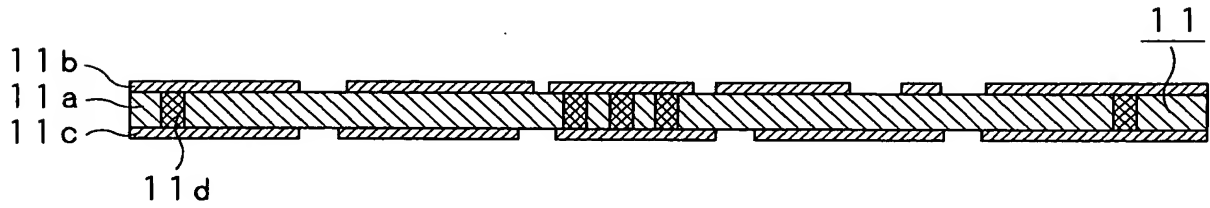


FIG. 5

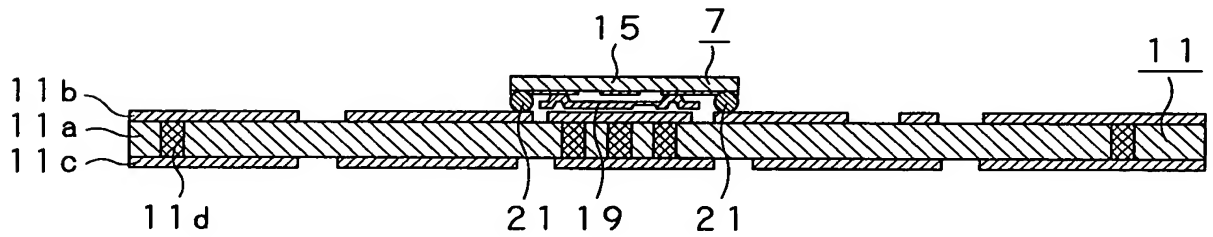


FIG. 6

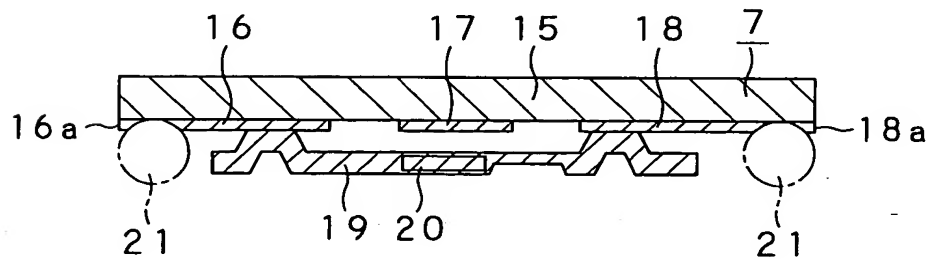


FIG. 7

5/11

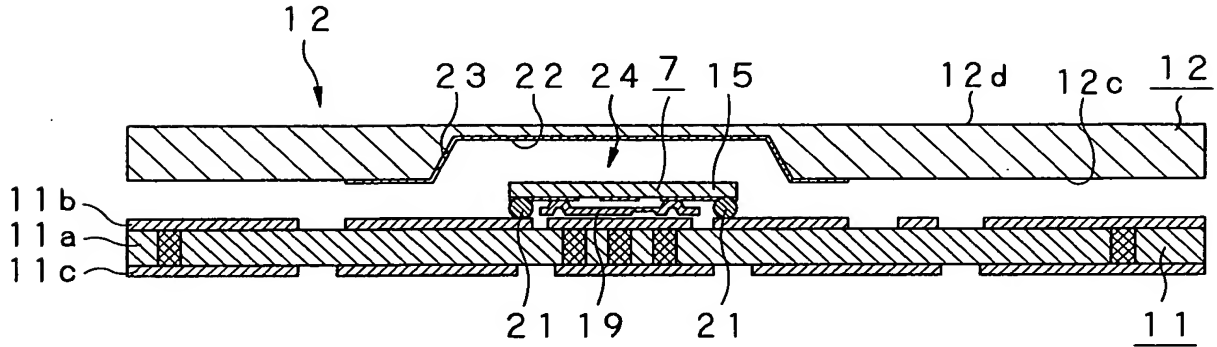


FIG. 8

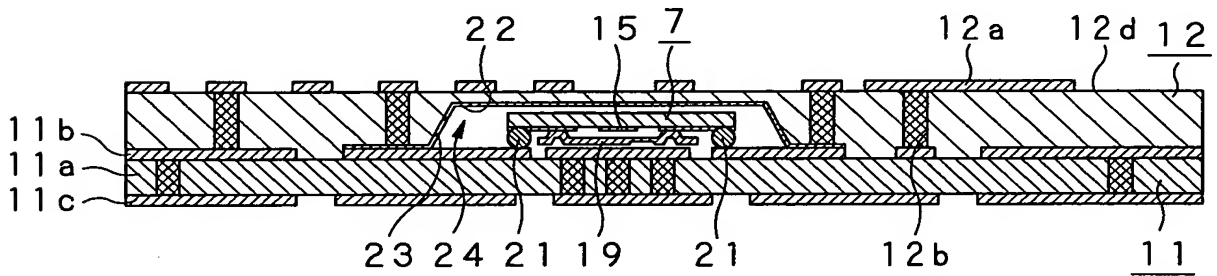


FIG. 9

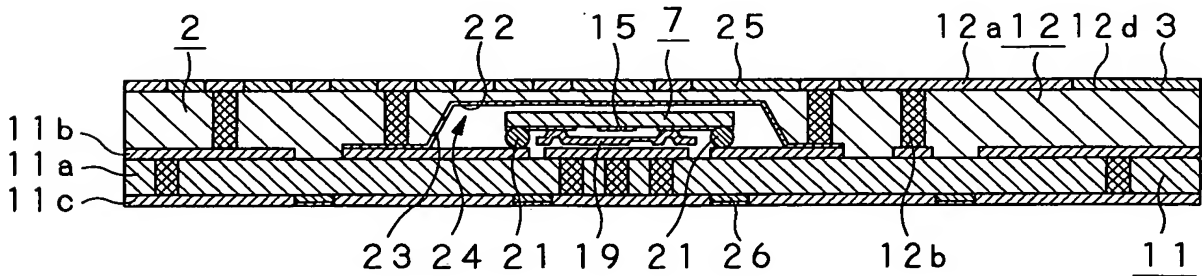


FIG. 10

6/11

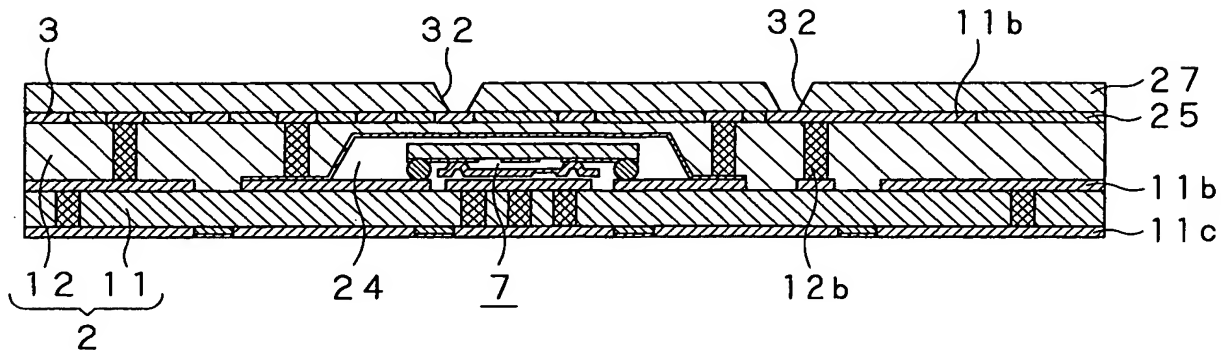


FIG. 1 1

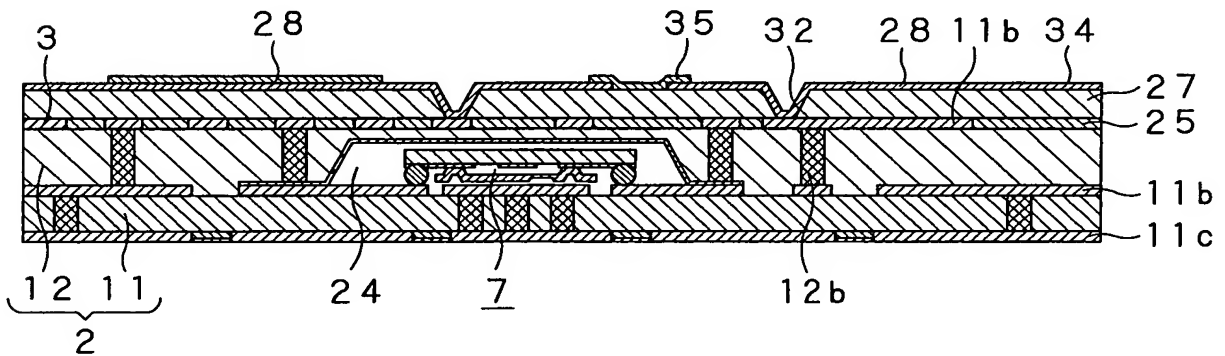


FIG. 1 2

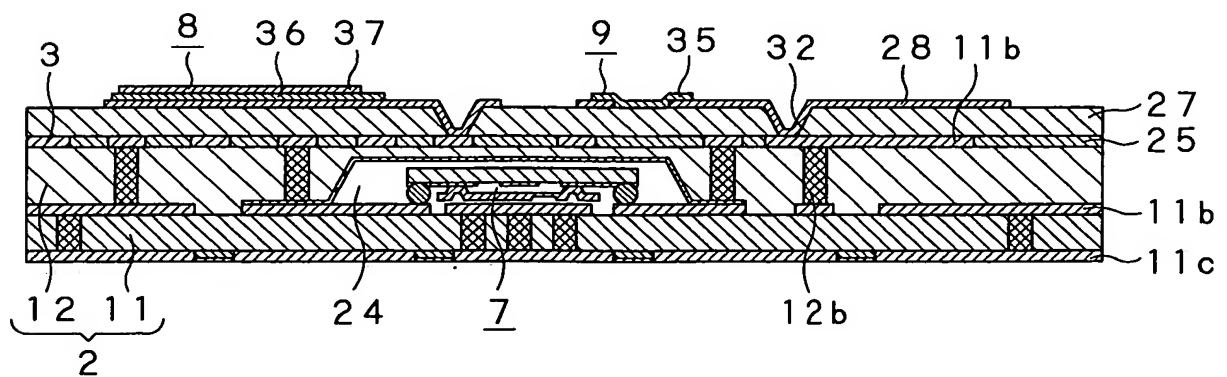


FIG. 13

7/11

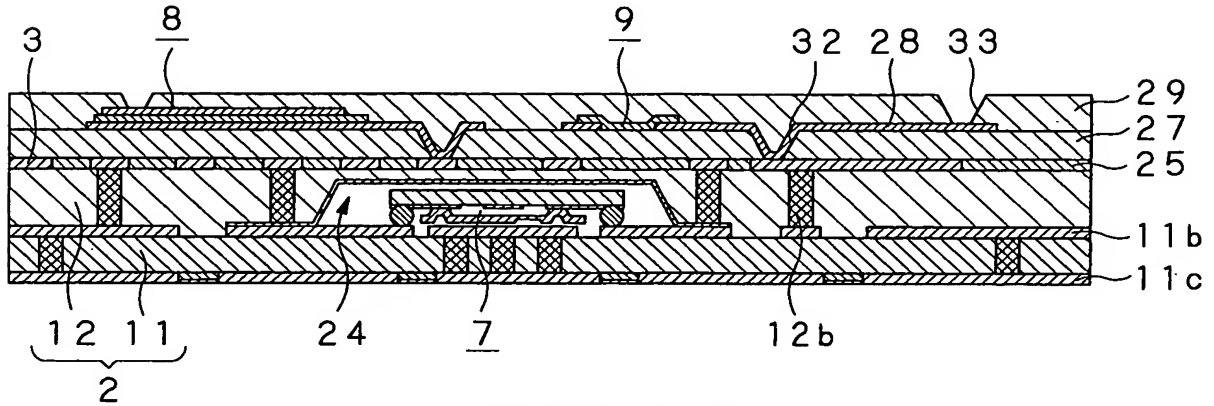


FIG. 14

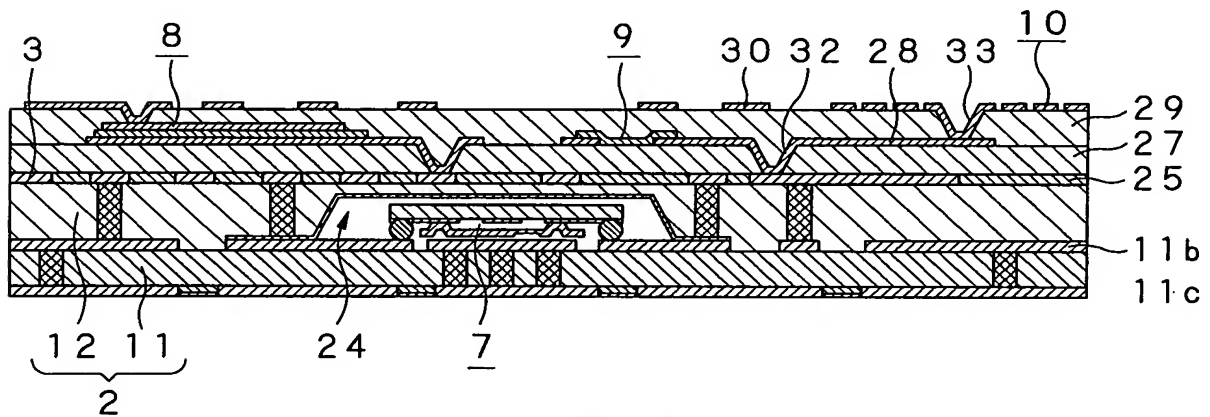


FIG. 15

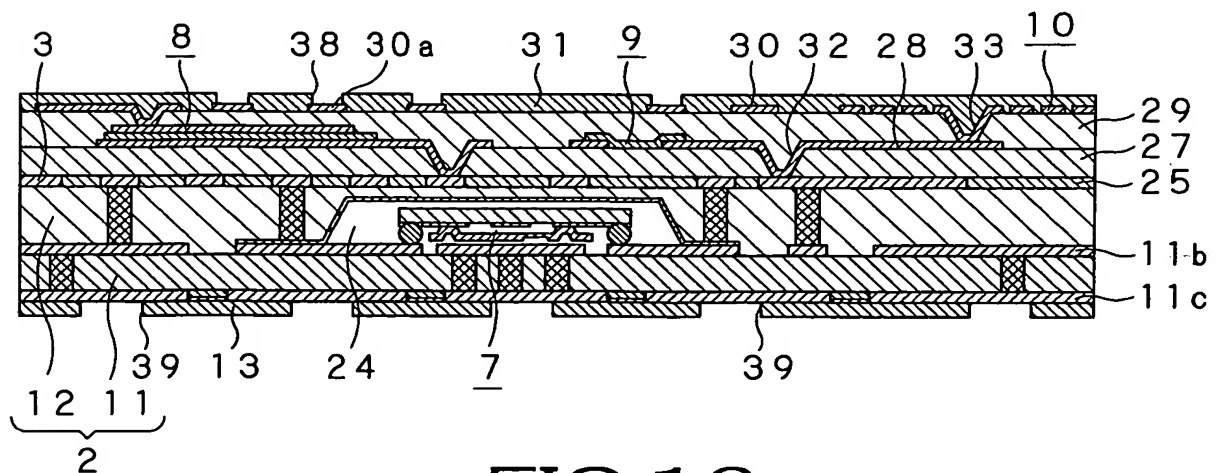


FIG. 16

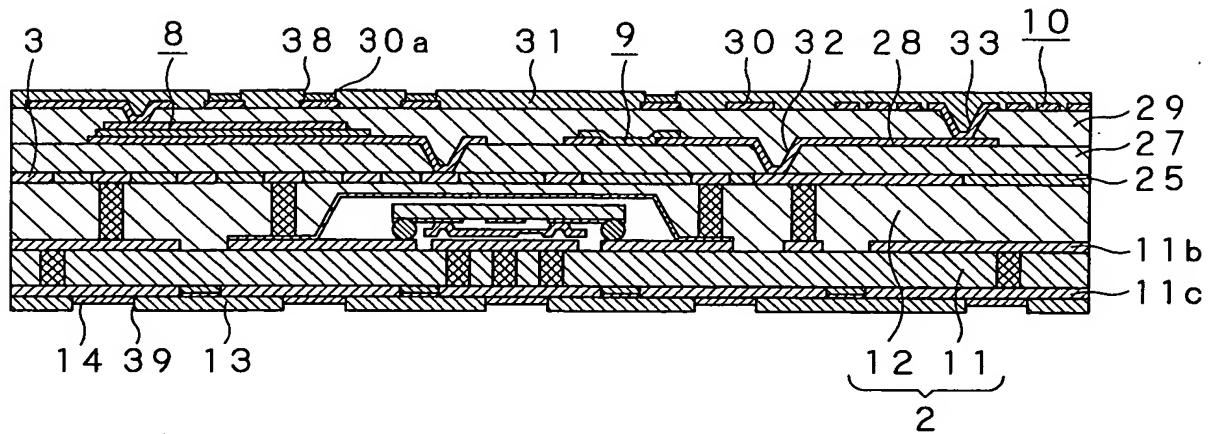


FIG. 17

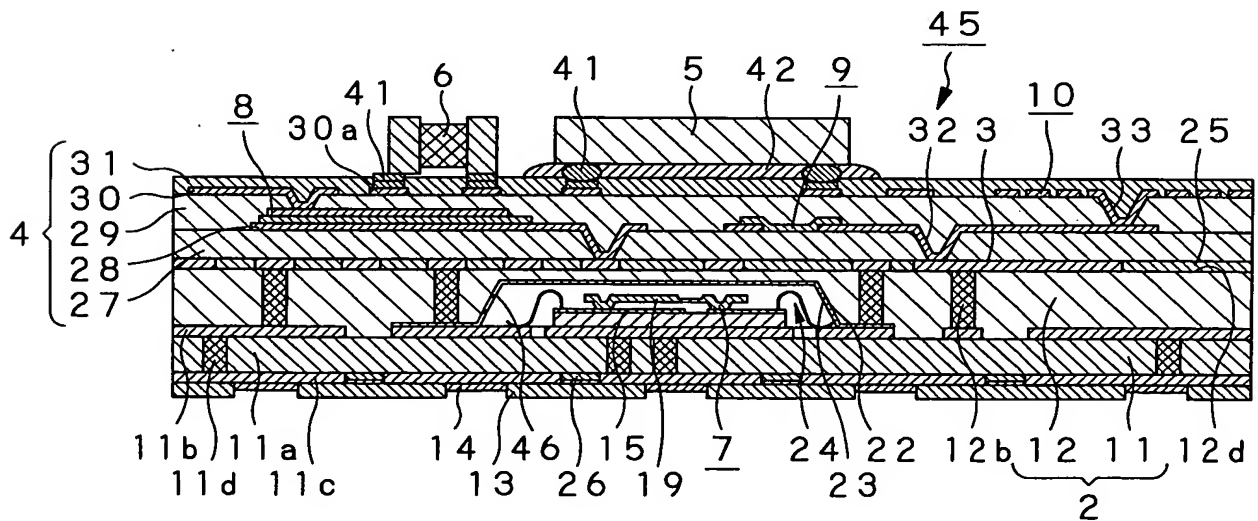


FIG. 18

A cross-sectional view of a semiconductor device 50. The device features a substrate 51 with a top layer 52. A central region 7 is defined by a trench 54 and a central block 55. The trench 54 is filled with a material 58. The central block 55 is surrounded by a material 59. The device is further defined by a layer 56 and a bottom layer 57. The device is divided into regions 11b and 11c. The device is labeled 50.

This cross-sectional view shows a substrate 51 with a top layer 52 and a bottom layer 51a. A central region 11b is defined by a top layer 11c and a bottom layer 11a. A side layer 51b is also shown.

FIG.21

10/11

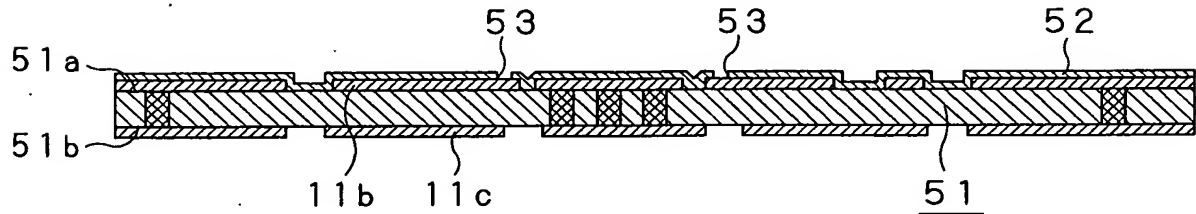


FIG. 22

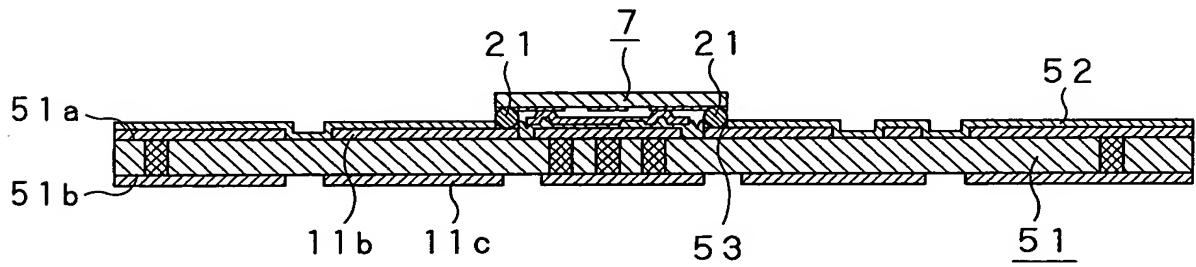


FIG. 23

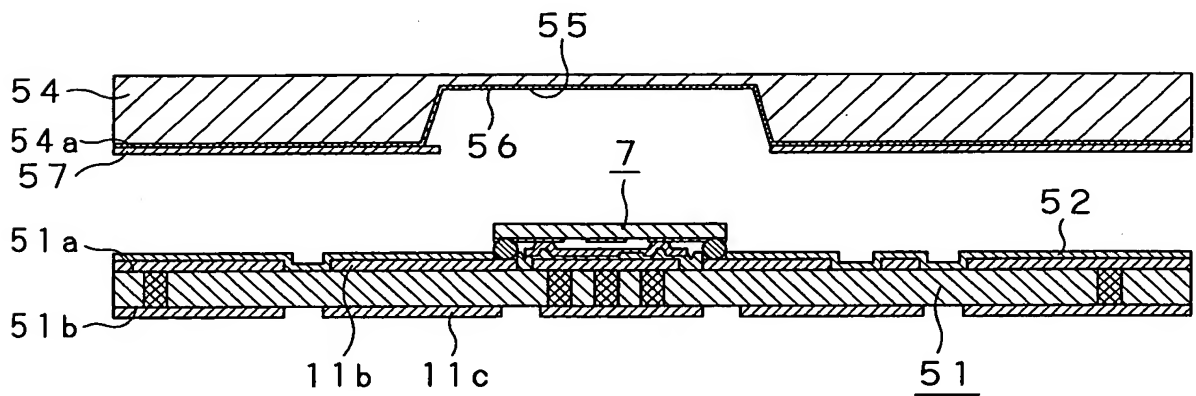


FIG. 24

11/11

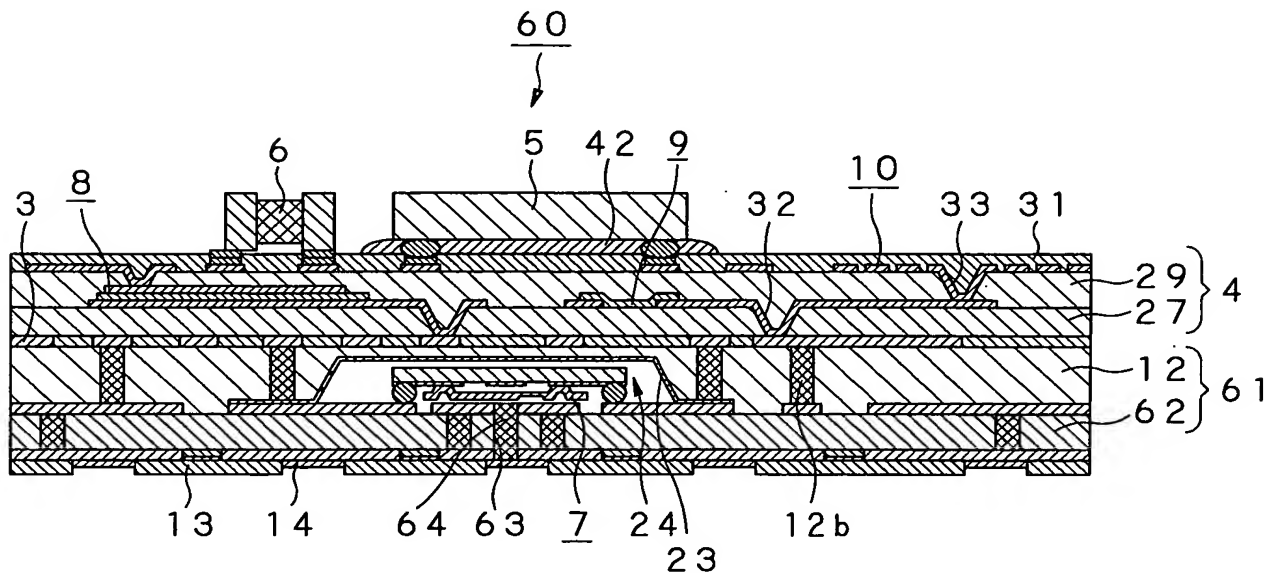


FIG. 25

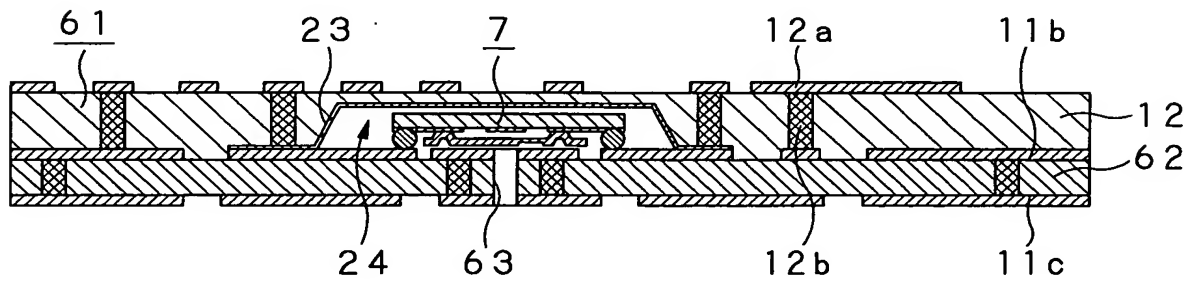


FIG. 26

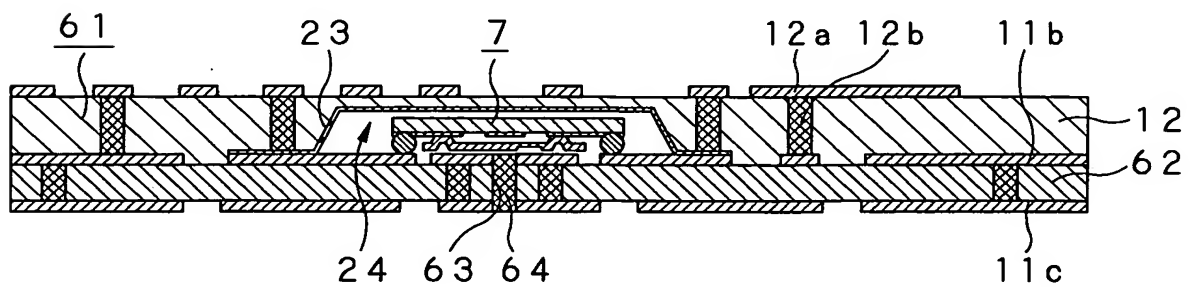


FIG.27